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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/661,287 | 09/12/2003 | Feng Chen | TI-35766 (032350.B524) | 7460 |

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| EXAMINER | |
|---|---|
| WILLIAMS, HOWARD L | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2819 | |

DATE MAILED: 01/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/661,287 | CHEN, FENG | |
| | Examiner | Art Unit | |
| | Howard L. Williams | 2819 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *31 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5,13 and 18-20* is/are allowed.

6)☒ Claim(s) *1-4,6-12 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

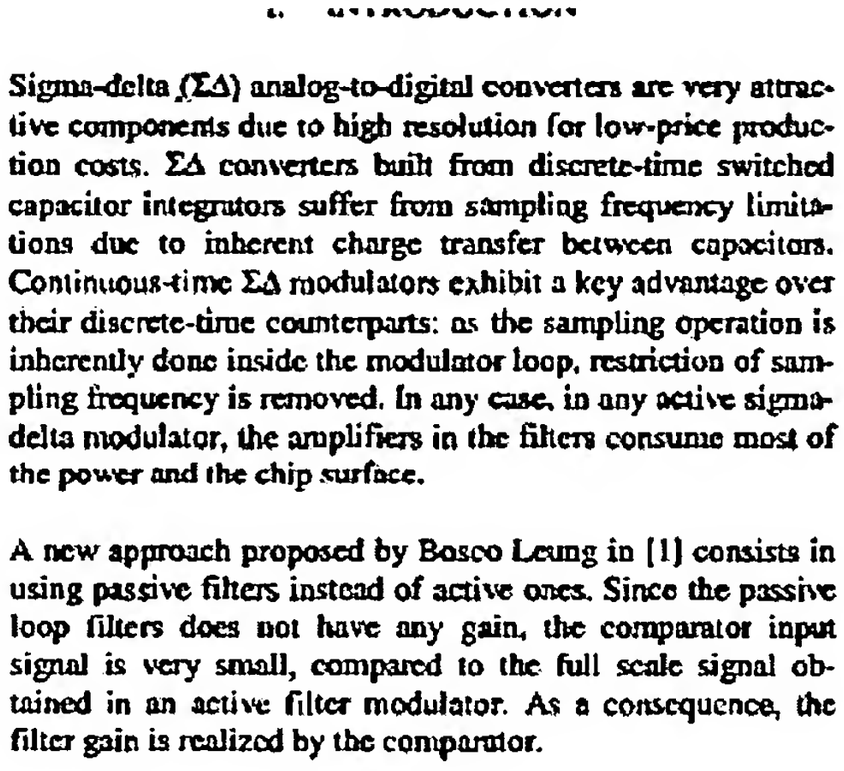
1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> *(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.*

Claims 1-4, 6-12, and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Benabes et al. article (*Passive sigma-delta converter design*) in view of the Chen et al. IEEE Journal of Solid State Circuits article (*A 0.25 mW 13 b passive ΣΔ modulator with a Built-In Mixer for a 10 MHz IF input*) and Yamakido et al. (US 5,227,795) or Voorman et al. (US 5,103,228). Benabes et al. article *Passive Sigma-Delta Converters Design* discloses a delta-sigma ADC with a continuous time passive filter (fig. 3 page 471). Benabes et al. also discloses a discrete time feedback circuit via the DAC shown in figure 1 (page 469). Benabes et al. shows in figure 2 a model of the feedback loop, input is taken as zero for figure 2, shown as a switch and hold element which is seen as reasonably suggestive of a capacitor for the hold element. Chen et al. discloses use of passive filtering delta-sigma ADC using switched capacitors in the feedback loop. Use of switched capacitor as the DAC feedback element in Benabes would have been obvious to provide a simple and compact DAC and the use of RC passive filters would provide reduced switching noise. Benabes et al. and Chen et al. don't specify whether the respective input signals are a voltage or a current signal so they don't disclose a transconductance element. Yamakido et al. and Voorman et al. disclose transconductance elements (V-I) to provide a current for summing with the fedback signal. The inclusion of a transconductance element in Benabes et al. would have been obvious because current summing is faster and more simply implemented than voltage summing.

Applicant's arguments filed 06 July 2005 have been fully considered but they are not persuasive. The remarks stress the passive discrete time filter in the feedback, arguing that the examiner's combination does not show passive filtering in both the feedforward path and feedback path. Benabes discloses passive filters in the first column and eschews amplifiers associated with the filters. Benabes does not disclose the filters as active as the remarks imply. From the introduction one would not read the use of any amplifier associated with a filter. Benabe's goal it seems is to use passive filters. Benabes shows in his figure 2 a switch and hold element (as a box) which can be readily implemented with a capacitor alone. Particularly where the goal is passive filters. Turning to the Chen article, it too shows passive discrete time feedback and a comparison with figure of the present application seems useful



Sigma-delta (ΣΔ) analog-to-digital converters are very attractive components due to high resolution for low-price production costs. ΣΔ converters built from discrete-time switched capacitor integrators suffer from sampling frequency limitations due to inherent charge transfer between capacitors. Continuous-time ΣΔ modulators exhibit a key advantage over their discrete-time counterparts: as the sampling operation is inherently done inside the modulator loop, restriction of sampling frequency is removed. In any case, in any active sigma-delta modulator, the amplifiers in the filters consume most of the power and the chip surface.

A new approach proposed by Bosco Leung in [1] consists in using passive filters instead of active ones. Since the passive loop filters does not have any gain, the comparator input signal is very small, compared to the full scale signal obtained in an active filter modulator. As a consequence, the filter gain is realized by the comparator.

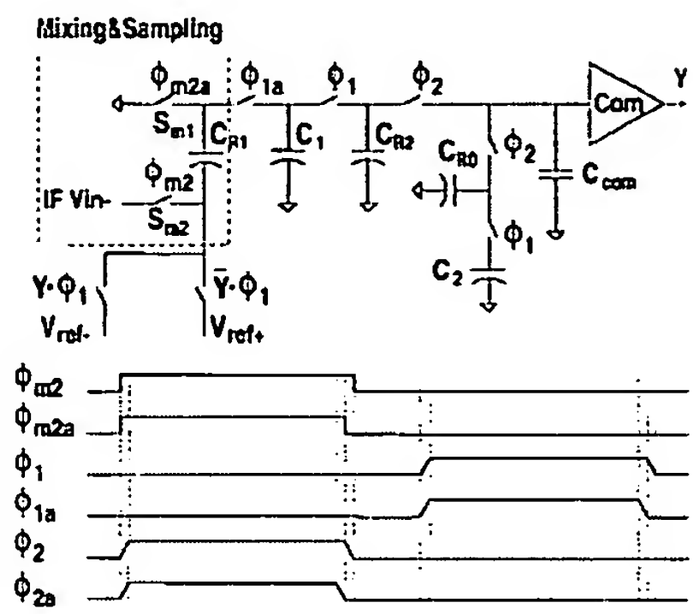



Fig. 8. A switched capacitor passive ΣΔ modulator with a built-in switch mixer.

Chen IEEE Journal Article figure 8.

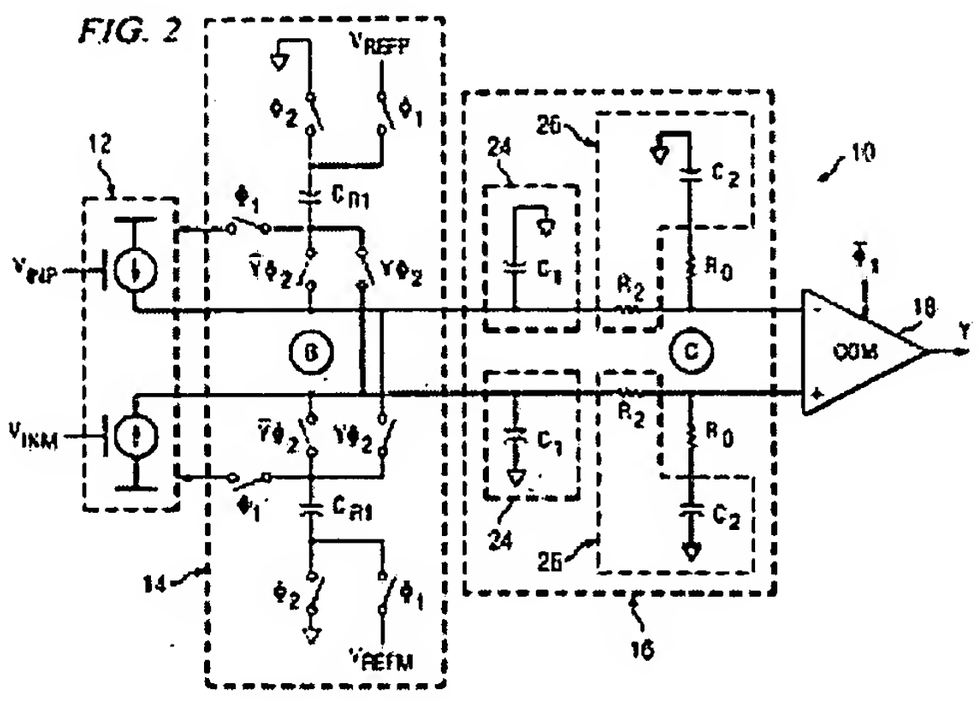



Figure 2 of present application.

While the Chen article uses a single line drawing in figure 8 the associated text on page 777 clearly states that it is one-half of a differential configuration.

Applicant's arguments filed 31 October 2005 have been fully considered but they are not persuasive. In yet another article seemingly authored by applicant it is made quite clear that the feedback path and loop filter are passive with the feedback path being discrete time. Benabes also uses discrete time feedback and a continuous time loop filter implemented with RC elements. The argument regarding the lack of discrete

time feedback to receive the feedback and the input is lacking because it does not matter how large the dashed line box 14 is drawn, it is still met by the references as they utilize DAC structures to provide the feedback and sum it with the input. The response also assails Benabes figures for showing what can be readily understood to be separate pieces that are connected together even if Benabes chose to illustrate them in separate figures.

Claims 5, 13 and 18-20 are allowable over the art of record which is not noted as disclosing the particular capacitance ratio recited in these claims.

Any inquiry concerning this communication should be directed to Howard L. Williams at telephone number 571.272.1815. The Patent and Trademark Office has a new central facsimile number for application specific correspondence intended for entry, it is 571-273-8300.

4 January 2006
Voice 571.272.1815

Howard L. Williams
Primary Examiner
Art Unit 2819